NSI-TEXE

NSITEXE NS31A FPGA User Manual

NSITEXE, Inc.

NRV31210052-00-E Revision 2.0.0 (Preliminary)

Index

About This Document

This document is a user manual for the NS31A FPGA.

It describes the hardware configuration and functional specifications for the NS31A FPGA and provides the information on how to use it.
The intended readers of this document are designers and programmers who develop NS31A using the NS31A FPGA.

Notices and Disclaimers

Chapter 1. Preparing to Use the NS31A FPGA

This chapter describes the hardware and software used by the NS31A FPGA.

For the functions and usage of the hardware and software described in this chapter, contact the relevant manufacturer or developer.

1.1. Hardware

The NS31A FPGA uses the hardware listed below.

Table 1. List of hardware used by the NS31A FPGA

Product name		Function
Arty-A7 Board		Board to integrate the NS31A FPGA.
Pmod peripheral module (option)	Pmod RTCC	Controls the real-time clock/calendar (RTCC) with a microchip (MCP79410) via the I2C interface. Two alarms can be set.
	Pmod SF3	Controls the 32-MB serial NOR flash memory via the SPI controller. It supports the extended SPI protocol, dual I/O, and quad I/O.
	Pmod MircoSD	Connected to the MicroSD card slot via the SPI controller. To exert control, insert the MicroSD card into the card slot. It supports 1-bit and 4-bit communication.
JTAG debugger (one of the products shown on the right)	IAR I-jet	Used to control the NS31A on the Arty-A7 board from the development PC. It controls the JTAG pins implemented on the Pmod connector, using the USB interface of the development PC.
	SEGGER J-Link	
	DLP DLP-USB1232H	
Others	USB cable	Interface cable used to connect the development PC and the Arty-A7 board.
	Development PC	Used for programming, debugging, etc.

Pmod is a low-frequency, small I/O interface board standard defined by Digilent, Inc. for connection between a host FPGA controller board and peripheral modules.
For details of Pmod, visit the website of Digilent, Inc.
http://store.digilentinc.com/pmod-modules/

1.2. Software

The NS31A FPGA uses the software listed below.

Table 2. List of software used by the NS31A FPGA

Tool	Product name	Verified version *1	Remarks
FPGA programmer	Xilinx Vivado	v2019.2.1	Used to rewrite Bitstream or Config ROM. For the writing method, please refer to the separate document “BIT file or Config ROM writing for Arty Board”.

Tool	Product name	Verified version *1	Remarks
JTAG control *2	IAR Embedded Workbench for RISC-V	v8.4	When IAR I-jet is used
	SEGGER Ozone	v3.22b	When SEGGER J-Link is used
	OpenOCD	v0.12.0	When DLP DLP-USB1232H is used *3
	GDB	13.0.50.20220805	When DLP DLP-USB1232H is used *3

*1 Version whose operation has been verified by NSITEXE, Inc.

*2 The tool to be used differs depending on the JTAG debugger used.

*3 When DLP-USB1232H is used, OpenOCD and GDB are used in combination.

1.3. Name of each part of the NS31A FPGA board

The names of the individual parts of the NS31A FPGA board (Arty-A7 board) that integrates NS31A are shown below.

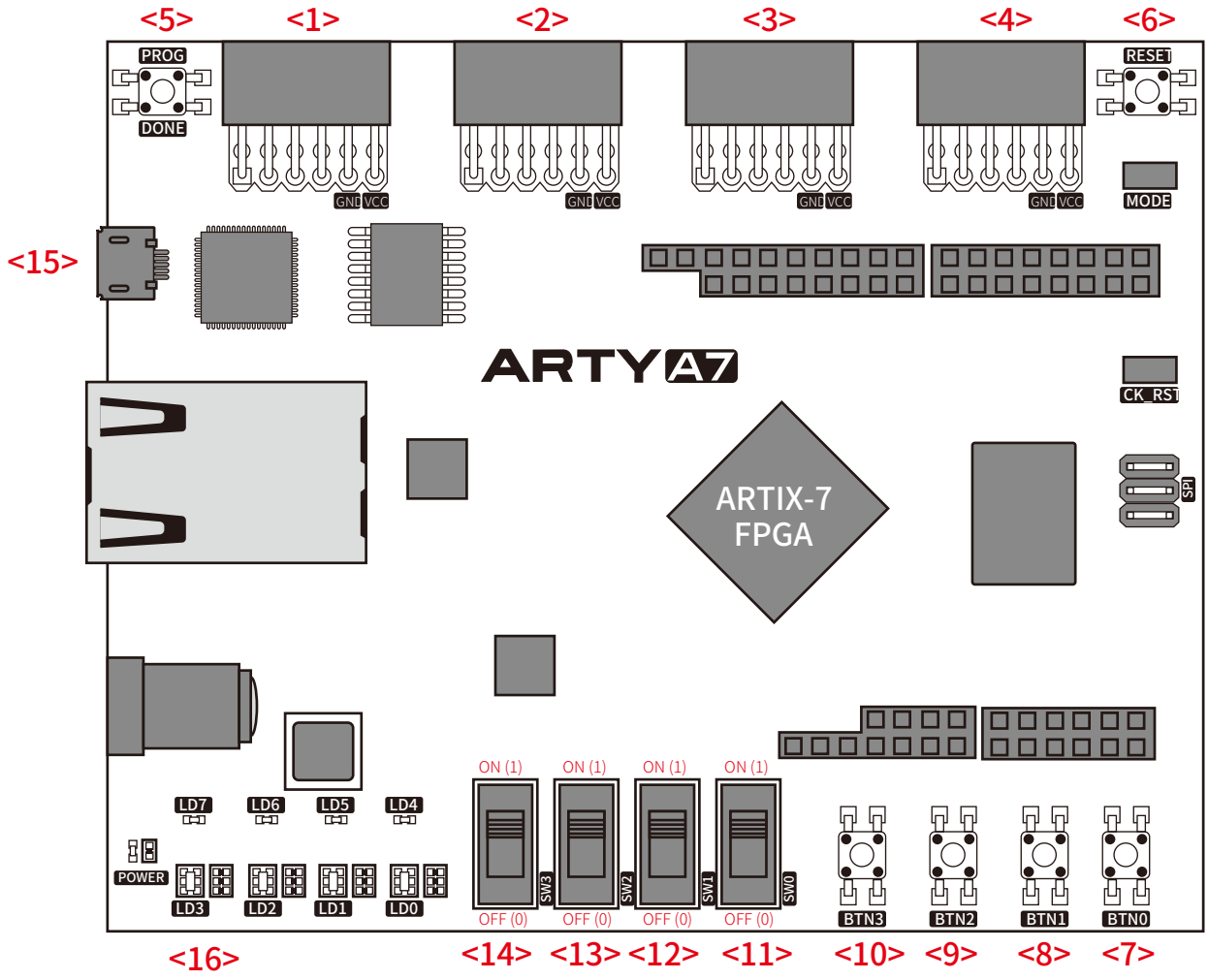


Figure 1. NS31A FPGA board Top View

Table 3. Name of each part of the NS31A FPGA

Name		Function
<1>	Pmod connector JA	Connects the Pmod RTCC. (Option)
<2>	Pmod connector JB	Connects the Pmod SF3. (Option)
<3>	Pmod connector JC	Connects the Pmod MicroSD slot. (Option)
<4>	Pmod connector JD	Connects the USB cable via an adapter to control the JTAG debugger, such as I-jet of IAR Systems.
<5>	PROG button	FPGA reconfiguration
<6>	RESET button	NS31A all reset (power-on reset)
<7>	BTN0 button	RV CPUSS Boot (NS31A Boot)
<8>	BTN1 button	Not used
<9>	BTN2 button	Not used
<10>	BTN3 button	Not used

Name		Function
<11>	SW0 switch	NS31A Reset Vector [SW1:SW0] 11 : Reserved region 10 : SPI0 Flash (Pmod SF3 XiP IF) 01 : ILM 00 : ZSBL ROM (not available)
<12>	SW1 switch	
<13>	SW2 switch	NS31A Boot Mode 1 : Boot (boot NS31A automatically after FPGA power-on)(recommend setting) 0 : No Boot (boot NS31A according to the NS31A register setting or by pressing BTN0)
<14>	SW3 switch	Boot ROM SPI selection 0 : SPI-Flash (When using this, be sure to set 0.) 1 : Reserved
<15>	USB connector	Connected to the UART in the Artix-7 control JTAG and NS31A FPGA via the FT2232 on the Arty-A7. Connect it to the USB connector of the development PC.
<16>	LED0~LED7	These LEDs are controlled via the GPIO controller.

Chapter 2. NS31A FPGA Overview

2.1. NS31A FPGA Block Daiagram

The following shows a block diagram of the NS31A FPGA.

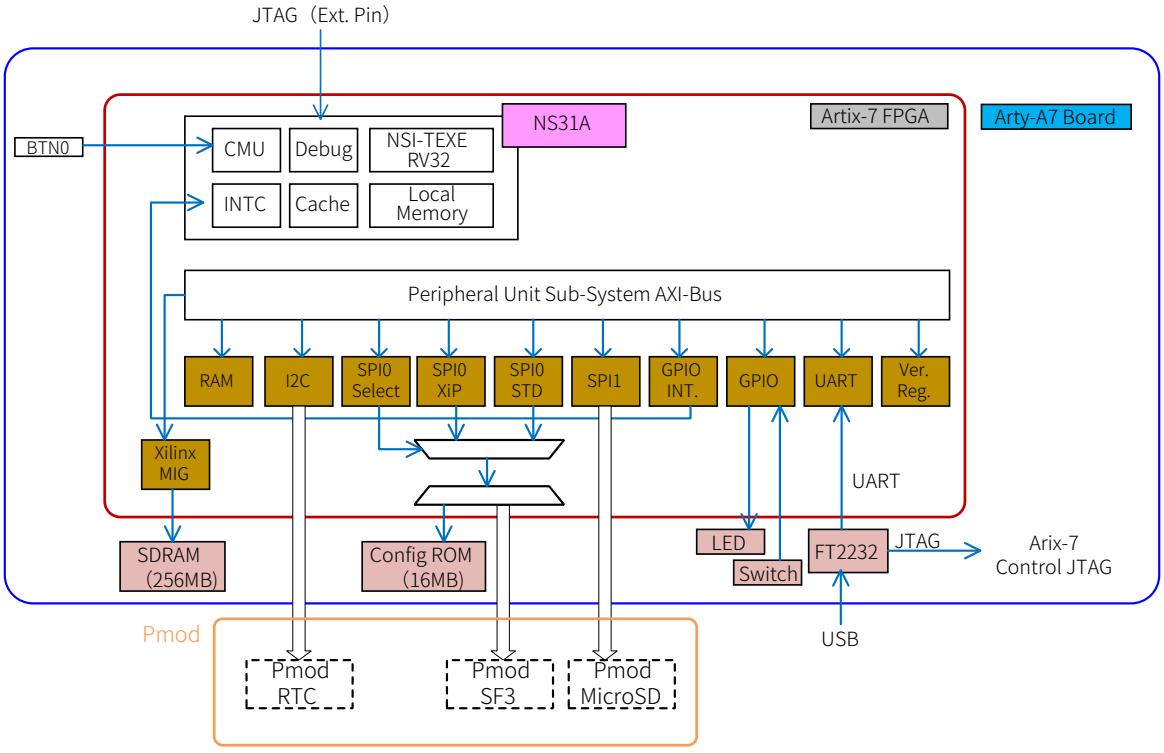


Figure 2. Block Diagram of NS31A FPGA

2.2. Features

The NS31A FPGA has the following features.

- NS31A
  RISC-V processor manufactured by NSITEXE, Inc.
- I2C RTC
  Controls the Pmod-connected RTCC using the IIC controller.
- SPI0 Flash
  Controls the Pmod-connected SF3 using the Quad SPI.
- SPI SD Card
  Controls the Pmod-connected MicroSD using the Quad SPI.
- GPIO
  Outputs an 8-bit GPIO signal to the LEDs using the GPIO.

- GPIO INT
  Outputs an interrupt to the CPUSS using the GPIO.
- Version Register
  Manages the RTL version information using the GPIO.

2.3. Clock, Reset

The operating clock of the NS31A CPU and peripheral modules is 25MHz. The NS31A FPGA reset is shown below.

- TRST(JTAG)
  Control the NS31A reset input pin jtag_trst_n to reset the DBG JTAG TAP module.
- nRST(JTAG) and RESET button
  Controls and resets the NS31A reset input terminals rst_pon and rst_sys. Reset the peripherals at the same time.
- System reset request defined in RISC-V architecture
  Controls the NS31A reset input terminal rst_sys.

For reset range of TRST, rst_pon and rst_sys, refer to NS31A UM 5.2 Reset section.

Chapter 3. Connecting the NS31A FPGA

3.1. Connecting to the JATG debugger and development PC

This section describes how to connect the Arty-A7 board to the JTAG debugger and development PC, as well as the pin assignment of the Pmod connector used to connect the JTAG debugger.

3.1.1. When IAR I-jet or SEGGER J-Link is used

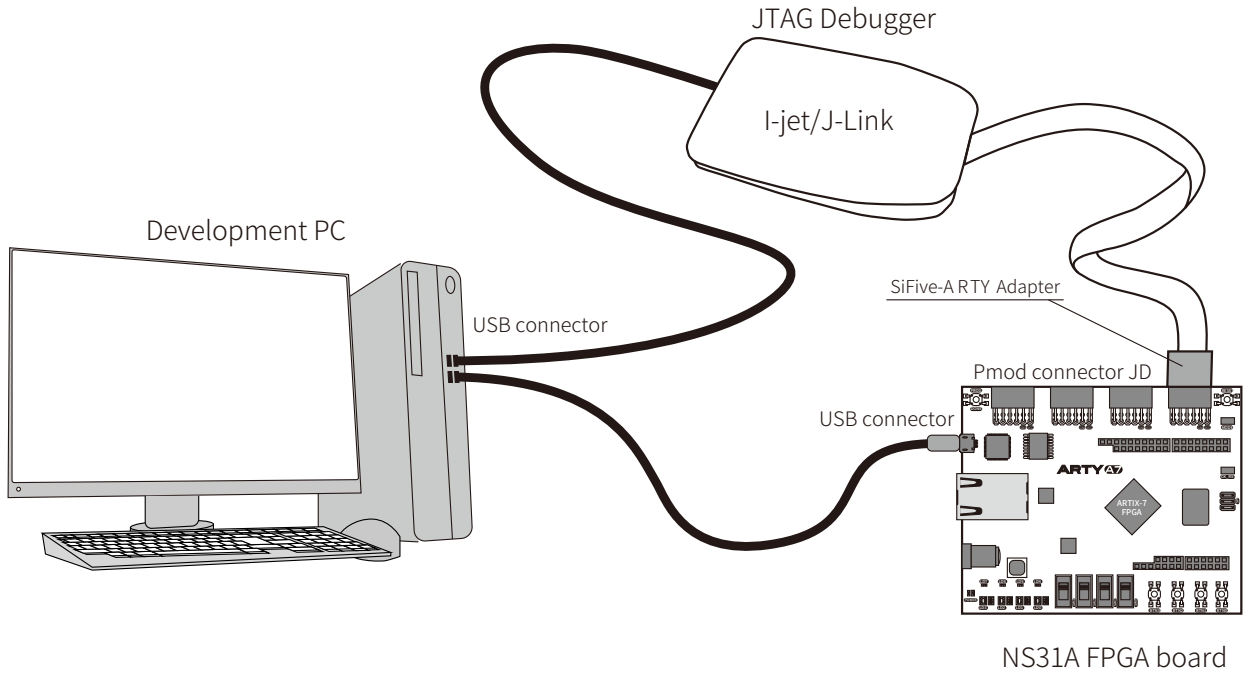
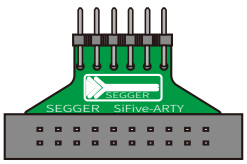


Figure 3. JTAG debugger connection diagram (I-jet/J-Link)

Connect the SEGGER SiFive-ARTY conversion board to the Pmod connector JD to use the 2.54-mm pitch, 20-pin connector. The following figure shows the pin assignment on the SEGGER SiFive-ARTY board side and JTAG side.

NS31A FPGA board side

6	5	4	3	2	1
VDD	GND	-	TCK	TRST	TDO
12	11	10	9	8	7
VDD	GND	-	nRST	TMS	TDI



JTAG Debugger side

19	17	15	13	11	9	7	5	3	1
–	–	–	TDO	–	TCK	TMS	TDI	–	–
20	18	16	14	12	10	8	6	4	2
GND	–	–	–	–	–	–	–	–	–

Figure 4. SEGGER SiFive-ARTY adapter pin assignment

3.1.2. When DLP-USB1232H is used

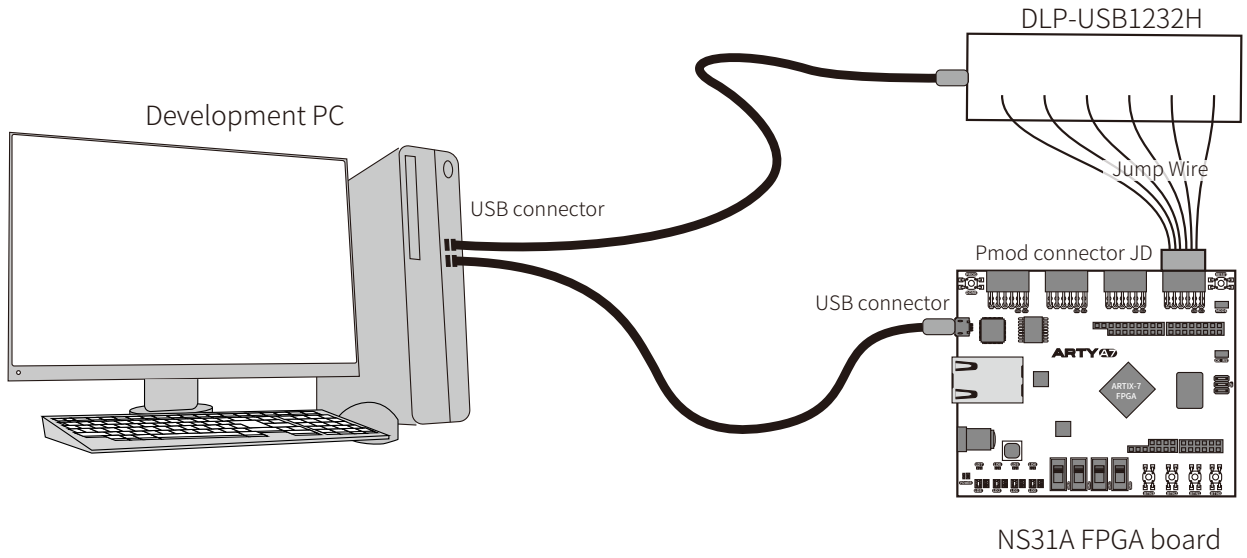


Figure 5. JTAG debugger connection diagram (DLP-USB1232H)

When DLP-USB1232H is used, connect it to the NS31A FPGA board using jump wires. The following figure shows the pin assignment adopted when DLP-USB1232H is used.

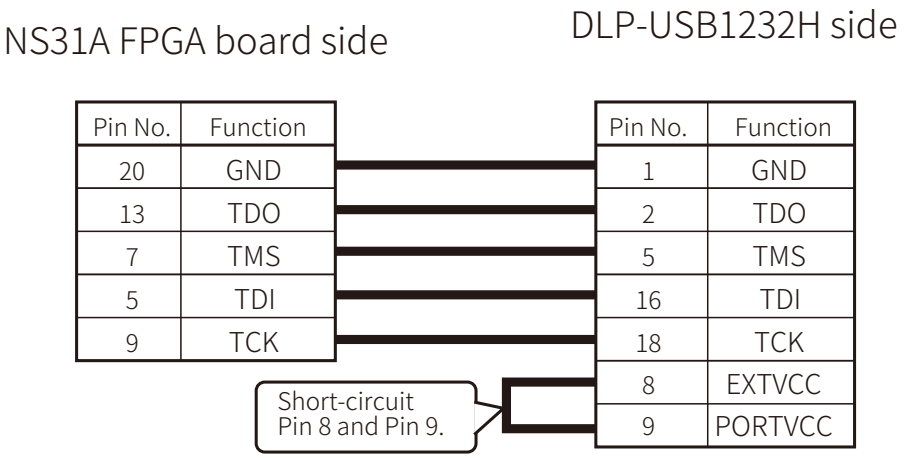


Figure 6. Connection of SEGGER SiFive-ARTY adapter and DLP-USB1232H

The power is supplied from pin 9 to the chip on DLP-USB1232H. Short-circuit pins 8 and 9 to supply the power from the USB terminal of DLP-USB1232H to the chip.

Chapter 4. Memory Map

4.1. System Memory Map

Table 4. System Memory Map

Start Address	End Address	Group	Region	Size
0000_0000H	0000_3FFFH	RV CPUSS	NS31A Debug Register	16KB
0000_4000H	0000_7FFFH	RV CPUSS	**Reserved**	
0000_8000H	0000_FFFFH	RV CPUSS	NS31A Hart Context Register	32KB
0001_0000H	017F_FFFFH	RV CPUSS	**Reserved**	
0180_0000H	0181_FFFFH	RV CPUSS	NS31A Instruction Local Memory (ILM)	128KB
0182_0000H	01FF_FFFFH	RV CPUSS	**Reserved**	
0200_0000H	0200_FFFFH	RV CPUSS	NS31A Internal Register (ACLINT)	64KB
0201_0000H	020F_FFFFH	RV CPUSS	**Reserved**	
0210_0000H	0210_0FFFH	RV CPUSS	NS31A Internal Register (CMU)	4KB
0210_1000H	0210_1FFFH	RV CPUSS	NS31A Internal Register (EM,LL,ICC,BP)	4KB
0211_0000H	0BFF_FFFFH	RV CPUSS	**Reserved**	
0C00_0000H	0C3F_FFFFH	RV CPUSS	NS31A Internal Register (PLIC)	4MB
0C40_0000H	1FFF_FFFFH	RV CPUSS	**Reserved**	
2000_0000H	200F_FFFFH	RV CPUSS	NS31A External Peripheral Bus (Not Used)	1MB
2010_0000H	3FFF_FFFFH	RV CPUSS	**Reserved**	
4000_0000H	41FF_FFFFH	Peripheral Unit	SPI0 XiP (Pmod SF3 direct address map)	32MB
4200_0000H	5FFF_FFFFH	Peripheral Unit	**Reserved**	
6000_0000H	6FFF_FFFFH	Peripheral Unit	DDR3 SDRAM	256MB
7000_0000H	7000_FFFFH	RV CPUSS	NS31A Data Local Memory (DLM)	64KB
7001_0000H	DFFF_FFFFH	RV CPUSS	**Reserved**	
E000_0000H	E000_0FFFH	Peripheral Unit (Exposure)	GPIO INT	4KB
E000_1000H	E1FF_EFFFH	Peripheral Unit	**Reserved**	
E1FF_F000H	E1FF_FFFFH	Peripheral Unit	Version Register	4KB
E200_0000H	E3FF_FFFFH	Peripheral Unit	**Reserved**	
E400_0000H	E400_0FFFH	Peripheral Unit	SPI0 Select	4KB
E400_1000H	E400_1FFFH	Peripheral Unit	GPIO	4KB
E400_2000H	E400_2FFFH	Peripheral Unit	I2C RTC	4KB
E400_3000H	E400_3FFFH	Peripheral Unit	SPI0 XiP (register region)	4KB
E400_4000H	E400_4FFFH	Peripheral Unit	SPI0 STD (standard read/write mode region)	4KB
E400_5000H	E400_5FFFH	Peripheral Unit	SPI1 (Micro SD)	4KB
E400_6000H	E400_6FFFH	Peripheral Unit	UART	4KB
E400_7000H	E87F_FFFFH	Peripheral Unit	**Reserved**	
E880_0000H	E880_FFFFH	Peripheral Unit	FPGA internal RAM 0	64KB
E881_0000H	E88F_FFFFH	Peripheral Unit	**Reserved**	
E890_0000H	E890_FFFFH	Peripheral Unit	FPGA internal RAM 1	64KB

Start Address	End Address	Group	Region	Size
E891_0000H	FFFF_FFFFH	Peripheral Unit	**Reserved**	

4.2. SDRAM

The following table shows the information about the SDRAM that can be connected to this product.

Table 5. SDRAM

Model	DDR3L SDRAM
Part number	MT41K128M16JT-125
Supply voltage	1.35 V
Size	256 MB
Data bus width	16 bits
Data rate	667 Mbps

- Details of the FPGA memory interface performance: See the Xilinx data sheet UG586 (Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions).
- Detailed specifications of DDR3L SDRAM: See the Micron Technology data sheet (CCMTD-1725822587-7895).

SDRAM is accessed via the Xilinx 7series MIG. Since SDRAM is automatically initialized after the reset is released, it does not need to be initialized by software.

Chapter 5. FPGA Logic

5.1. Overview

This FPGA Logic has a CPU and peripheral modules mounted on it.
Some of the peripheral modules use the Xilinx IP for boot control, interrupt control, Pmod control, etc.

5.2. CPU

As the CPU, NSITEXE NS31A is mounted. For details, see NS31A User Manual.
The operating clock of the CPU is 25MHz.
The operating clock of Machine Counter/Timers and User Counter/Timers listed in Table 14 .NS31A CSR List is also 25MHz.
The operating clock of MTIME_L/_H listed in Table 15 .NS31A FPGA Peripheral Register is also 25MHz.

5.2.1. Configuration Parameter List

The following table lists the configuration parameters of NS31A.

Table 6. Parameter List

Parameter	Value	Description
P_HARTID	0000 0000H	Specifies the hart ID.
P_CACHE_SIZE_IC	3	Instruction cache size 3: 16 KB
P_ADDR_BASE_ILM	0180 0000H	ILM base address
P_ADDR_SIZE_ILM	6	ILM size 6: 128 KB
P_ADDR_BASE_DLM	7000 0000H	DLM base address
P_ADDR_SIZE_DLM	5	DLM size 5: 64 KB
P_ADDR_BASE_DBG	0000 0000H	Debug register base address
P_ADDR_BASE_HCR	0000 8000H	Hart context register region base address
P_ADDR_BASE_ACLINT	0200 0000H	ACLINT Register Region base address
P_ADDR_BASE_CMU	0210 0000H	CMU Register Region base address
P_ADDR_BASE_REG	0210 1000H	Internal Register Region base address
P_ADDR_BASE_PLIC	0C00 0000H	PLIC Register Region base address
P_ADDR_BASE_PER	2000 0000H	External peripheral bus region base address (not used)
P_ADDR_SIZE_PER	9	External peripheral bus region size (not used) 9: 1 MB
P_BUS_PROT0_PRIV	0	Bus Access Privileged
P_RV32B	1	RV32B instruction support
P_RV32C	1	RV32C instruction support
P_BTB	0	BTB support
P_FPU	1	RV32F instruction support

Parameter	Value	Description
P_FPU_EXP2LOG2	0	Support of unique additional instructions (ns.fexp2.s and ns.flog2.s)
P_EXTINT_WIDTH	127	External interrupt input width
P_EXTINT_PRIWIDTH	4	External interrupt priority bit width from the outside
P_EXTINT_EDGE	all 1	select Edge/Level detection for external interrupt input

5.2.2. External interrupt input

The following table lists the NS31A external interrupt factors.

Table 7. Interrupt factor list

Factor	Connected destination
I2C RTC	External Interrupt[12]
SPI0 Flash	External Interrupt[11]
SPI1 MicroSD	External Interrupt[10]
UART	External Interrupt[9]
GPIO INT(ch1[7:0])	External Interrupt[8:1]
GPIO INT(ch2[0])	External NMI

5.2.3. Handling LR/SC/AMO

Use the NS31A internal memory area when using the AMO and LR/SC instructions.

5.3. SPI0 Select

The SPI0 Select module enables the SPI0 Flash mode selection by using Xilinx's GPIO controller [Xilinx IP: AXI GPIO v2.0].

Table 8. SPI0 Select module overview

Base Address	Channel	Overview	Setting value
E400_0000H	1	SPI0 communication mode selector	[0] Reserved [1] SPI0 Mode Select 0: XiP (high-speed read) mode (default) 1: STD (standard read/write) mode [31:2] Reserved

For details of [Xilinx IP: AXI GPIO v2.0], see the corresponding data sheet.

5.4. I2C RTC

The I2C RTC module controls the external Pmod RTCC via Xilinx's I2C IP [Xilinx IP: AXI IIC Bus Interface v2.0].
I2C provides two low-speed serial bus interfaces (clock/data) to the external Pmod RTC.

- The base address is E400 2000H.

The I2C controller module is a bus controller capable of operating as the master and supports the 100-kbps clock

frequency. This controller supports the 7-bit address mode. When data is received, it can also notify the processor by using a data interrupt or transfer complete interrupt.
The clock frequencies of up to 100 kHz of the I2C clock (scl) are supported.

For details of the I2C controller features and registers, see the Xilinx data sheet (pg090).

5.5. SPI0 Flash

The SPI0 Flash module controls the external Pmod SPI SF3 (32 MB serial NOR flash memory) via Xilinx's SPI controller [Xilinx IP: AXI Quad SPI v3.2].
SPI SF3 provides four serial bus interfaces (clock/TX data/RX data/slave select).
The SPI controller module supports clock frequencies of up to 50 MHz.

SPI0 Select enables you to select either the XiP (high-speed read) mode or the STD (standard read/write) mode. For details of SPI0 Select, see Section 5.3. The following table provides an overview of each mode.

Table 9. SPI0 Flash mode overview

Mode	Region	Base Address
XiP mode (default)	High-speed read mode region	4000 0000H
	Register region	E400 3000H
STD mode	Standard read/write mode, register region	E400 4000H

The two modes cannot be used at the same time. Be sure to access the area corresponding to the mode selected with SPI0 Select.

5.5.1. XiP (high-speed read) mode

This is one of the SPI0 Flash control modes. The XiP mode has the following features.

- The clock polarity (CPOL) or clock phase (CPHA) setting can be changed by accessing the configuration register using the AXI4-Lite interface.
- The external flash memory data can be read by using three high-speed read commands according to the configuration mode.
    - High-speed read (0BH)
    - High-speed read dual I/O (BBH)
    - High-speed read quad I/O (EBH)
- In this implementation, the configuration mode is set to the high-speed read mode.

5.5.2. STD (standard read/write) mode

This is one of the SPI0 Flash control modes. The STD mode has the following features.

- The SPI core uses the AXI4-Lite interface only.

- The flash memory data can be written, read, and deleted by configuring the relevant command register settings.
- It is possible to use 16 dedicated FIFO buffer (TXFIFO/RXFIFO) stages for the data write and read operations, respectively.

For details of the SPI controller features and registers, see the Xilinx data sheet (pg153).

5.6. SPI1 MicroSD

The SPI1 MicroSD module controls the MicroSD connected to the external Pmod MicroSD slot via Xilinx's SPI controller [Xilinx IP: AXI Quad SPI v3.2].
It provides four serial bus interfaces (clock/TX data/RX data/slave select) to the MicroSD.

- SPI1 uses the AXI4-Lite interface only.
- The base address is E400 5000H.
- The MicroSD data can be written, read, and deleted by configuring the relevant command register settings. It is possible to use 16 dedicated FIFO buffer (TXFIFO/RXFIFO) stages for the data write and read operations, respectively.

For details of the SPI controller features and registers, see the Xilinx data sheet (pg153).

5.7. GPIO

The GPIO module controls the GPIO via Xilinx's GPIO controller [Xilinx IP: AXI GPIO v2.0].
Each GPIO pin is connected to an LED on the NS31A FPGA board.

For details of the GPIO controller features and registers, see the Xilinx data sheet (pg144). Only channel 1 in the GPIO controller is used.

Details of the connected destination of each GPIO pin are given below.

The GPIO register has a 32-bit configuration, and eight of these bits are used for LED connection.

Table 10. GPIO module overview

Base Address	Width	Default		Connected destination	
		I/O	Value	Bit	Board
E400 1000H	[31:0]	Output	0000 0000H	[0]	LED0 Green
				[1]	LED1 Green
				[2]	LED2 Green
				[3]	LED3 Green
				[4]	LED4 Green
				[5]	LED5 Green
				[6]	LED6 Green
				[7]	LED7 Green
				[31:8]	Not used

5.8. LED

The LEDs on the board notify the user of the FPGA status. The following table shows what the individual LEDs notify.

Table 11. LED notification

LED	Control source	Notification content
LD0-B	MIG-DDR3	DDR3 calibration complete
LD0-G	GPIO	GPIO bit[0]
LD0-R	MIG DDR3	DDR3 Calibration Fail
LD1-B	reserve	-
LD1-G	GPIO	GPIO bit[1]
LD1-R	reserve	-
LD2-B	reserve	-
LD2-G	GPIO	GPIO bit[2]
LD2-R	reserve	-
LD3-B	reserve	-
LD3-G	GPIO	GPIO bit[3]
LD3-R	reserve	-
LD4	GPIO	GPIO bit[4]
LD5	GPIO	GPIO bit[5]
LD6	GPIO	GPIO bit[6]
LD7	GPIO	GPIO bit[7]

5.9. GPIO INT

The GPIO INT module outputs one NMI and eight interrupt factors to the RV CPU via Xilinx's GPIO controller [Xilinx IP: AXI GPIO v2.0].
For details of the GPIO controller features and registers, see the Xilinx data sheet (pg144).
Details of each interrupt factor are given below.

Table 12. GPIO INT module overview

Base Address	Channel	Default		Connected destination		Remarks
		I/O	Value	Bit	Module	
E000 0000H	1(INT)	output	0000 0000H	[7:0]	RV CPU	Level: High Active
				[31:8]	Not used	
E000 0008H	2(NMI)	output	0000 0000H	[0]	RV CPU	Level: High Active
				[31:1]	Not used	

5.10. UART

The UART module controls the JTAG debugger connected to the Pmod USBUART via Xilinx's UART Lite controller [Xilinx IP: AXI UART Lite v2.0]. It provides two serial bus interfaces (TX data/RX data) to the USBUART.
The base address is E400_6000H.
For details of the UART Lite controller features and registers, see the Xilinx data sheet (pg142).
The settings of the Xilinx IP: UART Lite controller are shown below.

- Data bits: 8
- Parity: None

The baud rate setting cannot be changed.
Baud rate: 9600

5.11. Version Register

The Version Registers provide the FPGA version information using Xilinx's GPIO controller [Xilinx IP: AXI GPIO v2.0]. (For debugging) For details of the GPIO controller features and registers, see the Xilinx data sheet (pg144). Only channel 1 in the GPIO controller is used.

Table 13. Version module overview

Address	Type	Name	Bit	Overview	Setting value
E1FF_F000H	RO	GPIO_DATA	[31:0]	Version register	[31:24] YEAR [23:16] MONTH [15:8] DAY [7: 0] REV
E1FF_F008H	RO	GPIO_DATA	[31:0]	Version register	[31:16] CPU Revision [15:0] FPGA Version/Revision

Chapter 6. Starting the NS31A FPGA

6.1. Starting sequence

This section describes an example of the starting sequence applicable when DLP-USB1232H and OpenOCD are used.

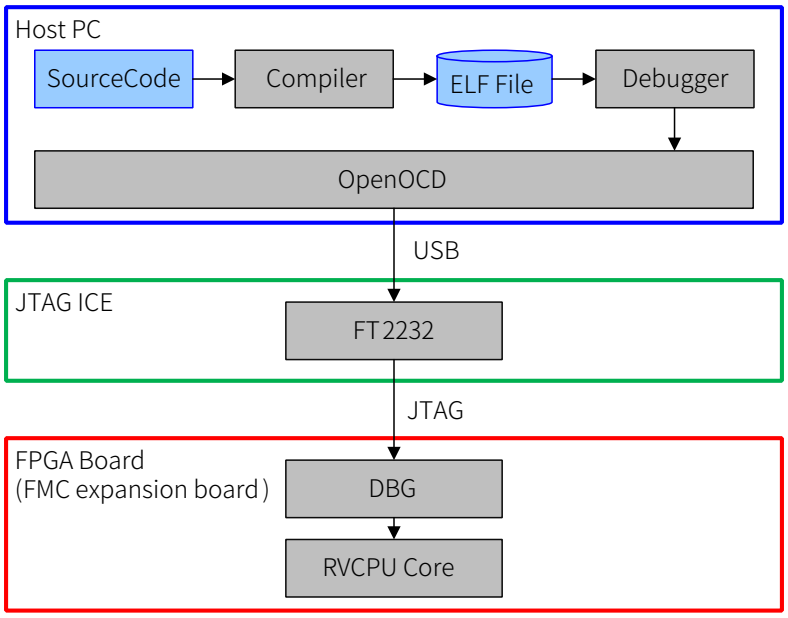


Figure 7. JTAG connection schematic diagram

■Start OpenOCD sample

Open a terminal window and launch OpenOCD.

```
$ sudo /opt/openocd/bin/openocd -c 'bindto 0.0.0.0' -f /opt/openocd/sample/akaria-ns31-arty-dlp-usb1232h.cfg
```

It will be in Running state without prompt.

The configuration sample files "akaria-ns31-arty-dlp-usb1232h.cfg" can be downloaded from NSITEXE Website.

■Start gdb sample

After starting OpenOCD, open another terminal window and start gdb.

```
$ /opt/riscv/riscv64-unknown-elf/bin/riscv64-unknown-elf-gdb sample_blink_led.elf
```

*"sample_blink_led.elf" is an example of an executable file.
Executing the above command enables JTAG access using gdb.

Appendix A: NS31A FPGA Register List

The following table lists the NS31A FPGA registers.

NS31A CSR(Control and Status Register) listed in Table 14 is a register for control and status acquisition, which is mapped to a unique address space, and dedicated access instructions are provided.

For details about each register, see the NSITEXE NS31A User Manual and the relevant Xilinx IP data sheets.

Table 14. NS31A CSR list

Region	Register Name	Register No.	Address
User Floating-Point CSRs	fflags	001H	-
User Floating-Point CSRs	frm	002H	-
User Floating-Point CSRs	fcsr	003H	-
Machine Trap Setup	mstatus	300H	-
Machine Trap Setup	misa	301H	-
Machine Trap Setup	mie	304H	-
Machine Trap Setup	mtvec	305H	-
Machine Counter Setup	mcounteren	306H	-
Machine Counter Setup	mcountinhibit	320H	-
Machine Trap Handling	mscratch	340H	-
Machine Trap Handling	mepc	341H	-
Machine Trap Handling	mcause	342H	-
Machine Trap Handling	mtval	343H	-
Machine Trap Handling	mip	344H	-
Machine Protection and Translation	pmpcfg0	3A0H	-
Machine Protection and Translation	pmpcfg1	3A1H	-
Machine Protection and Translation	pmpcfg2	3A2H	-
Machine Protection and Translation	pmpcfg3	3A3H	-
Machine Protection and Translation	pmpaddr0	3B0H	-
Machine Protection and Translation	pmpaddr1	3B1H	-
Machine Protection and Translation	pmpaddr2	3B2H	-
Machine Protection and Translation	pmpaddr3	3B3H	-
Machine Protection and Translation	pmpaddr4	3B4H	-
Machine Protection and Translation	pmpaddr5	3B5H	-
Machine Protection and Translation	pmpaddr6	3B6H	-
Machine Protection and Translation	pmpaddr7	3B7H	-
Machine Protection and Translation	pmpaddr8	3B8H	-
Machine Protection and Translation	pmpaddr9	3B9H	-
Machine Protection and Translation	pmpaddr10	3BAH	-
Machine Protection and Translation	pmpaddr11	3BBH	-
Machine Protection and Translation	pmpaddr12	3BCH	-
Machine Protection and Translation	pmpaddr13	3BDH	-

Region	Register Name	Register No.	Address
Machine Protection and Translation	pmpaddr14	3BEH	-
Machine Protection and Translation	pmpaddr15	3BFH	-
Debug/Trace registers	tselect	7A0H	-
Debug Mode Registers	tdata1	7A1H	-
Debug Mode Registers	tdata2	7A2H	-
Debug Mode Registers	tinfo	7A4H	-
Debug Mode Registers	dcsr	7B0H	-
Debug Mode Registers	dpc	7B1H	-
Debug Mode Registers	dscratch0	07B2H	-
Exception Error Address of first imprecise data access fault (NS31A Extended)	meecaddr	-	0000 9F0CH
Exception Error Address of first imprecise data access fault (NS31A Extended)	meecunlock	-	0000 9F10H
Machine Counter/Timers	mcycle	B00H	-
Machine Counter/Timers	minstret	B02H	-
Machine Counter/Timers	mcycleh	B80H	-
Machine Counter/Timers	minstreth	B82H	-
Hart control (NS31A Extended)	mhtpc	-	0000 AF00H
Hart control (NS31A Extended)	mhtenable	-	0000 AF40H
Hart control (NS31A Extended)	mhtstatus	-	0000 AF80H
L1 Instruction Cache control (NS31A Extended)	ml1cachesysctrl	-	0000 AFA0H
L1 Instruction Cache control (NS31A Extended)	ml1cacheoperation	-	0000 AFA4H
L1 Instruction Cache control (NS31A Extended)	ml1cacheprefcfg	-	0000 AFA8H
L1 Instruction Cache control (NS31A Extended)	mbpsysctrl	-	0000 AFB8H
L1 Instruction Cache control (NS31A Extended)	mbpoperation	-	0000 AFBCH
User Counter/Timers	cycle	C00H	-
User Counter/Timers	time	C01H	-
User Counter/Timers	instret	C02H	-
User Counter/Timers	cycleh	C80H	-
User Counter/Timers	timeh	C81H	-
User Counter/Timers	instreth	C82H	-
Machine Information Registers	mvendorid	F11H	-
Machine Information Registers	marchid	F12H	-
Machine Information Registers	mimpid	F13H	-
Machine Information Registers	mhartid	F14H	-
Hart Fetch address Register (NS31A Extended)	mhtfetchaddr	-	0000 BF00H

Table 15. NS31A FPGA Peripheral Register list

Region	Register Name	Address 1	Address 2
ACLINT	MTIME_L	0200 BFF8H	-
ACLINT	MTIME_H	0200 BFFCH	-
ACLINT	MTIMECMP_L	0200 4000H	-
ACLINT	MTIMECMP_H	0200 4004H	-
ACLINT	MTIMECTRL	0200 D000H	-
ACLINT	MSIP	0200 0000H	-
ACLINT	MTIMERCFG	0200 FF40H	-
ACLINT	MSWICFG	0200 FF00H	-
PLIC	EISPRI0	0C00 0000H	-
PLIC	EISPRI1	0C00 0004H	-
PLIC	EISPRI2	0C00 0008H	-
:	:	:	:
PLIC	EISPRI127	0C00 01FCH	-
PLIC	EISPEN0	0C00 1000H	-
PLIC	EISPEN1	0C00 1004H	-
PLIC	EISPEN2	0C00 1008H	-
PLIC	EISPEN3	0C00 100CH	-
PLIC	EISPEN4	0C00 1010H	-
PLIC	EISPEN5	0C00 1014H	-
PLIC	EISPEN6	0C00 1018H	-
PLIC	EISPEN7	0C00 101CH	-
PLIC	EIHMEN0	0C00 2000H	-
PLIC	EIHMEN1	0C00 2004H	-
PLIC	EIHMEN2	0C00 2008H	-
PLIC	EIHMEN3	0C00 200CH	-
PLIC	EIHMEN4	0C00 2010H	-
PLIC	EIHMEN5	0C00 2014H	-
PLIC	EIHMEN6	0C00 2018H	-
PLIC	EIHMEN7	0C00 201CH	-
PLIC	EISFSTAT0	0C1F 8000H	-
PLIC	EISFSTAT1	0C1F 8004H	-
PLIC	EISFSTAT2	0C1F 8008H	-
PLIC	EISFSTAT3	0C1F 800CH	-
PLIC	EISFSTAT4	0C1F 8010H	-
PLIC	EISFSTAT5	0C1F 8014H	-
PLIC	EISFSTAT6	0C1F 8018H	-
PLIC	EISFSTAT7	0C1F 801CH	-
PLIC	EISFCLR0	0C1F 9000H	-
PLIC	EISFCLR1	0C1F 9004H	-
PLIC	EISFCLR2	0C1F 9008H	-

Region	Register Name	Address 1	Address 2
PLIC	EISFCLR3	0C1F 900CH	-
PLIC	EISFCLR4	0C1F 9010H	-
PLIC	EISFCLR5	0C1F 9014H	-
PLIC	EISFCLR6	0C1F 9018H	-
PLIC	EISFCLR7	0C1F 901CH	-
PLIC	EICFGST0	0C1F C000H	-
PLIC	EICFGST1	0C1F C004H	-
PLIC	EICFGST2	0C1F C008H	-
PLIC	EICFGST3	0C1F C00CH	-
PLIC	EICFGST4	0C1F C010H	-
PLIC	EICFGST5	0C1F C014H	-
PLIC	EICFGST6	0C1F C018H	-
PLIC	EICFGST7	0C1F C01CH	-
PLIC	EICFGHI	0C1F D000H	-
PLIC	EIH0TH	0C20 0000H	-
PLIC	EIH0CID	0C20 0004H	-
CMU control register	STATSYS	0210 0200H	-
CMU control register	STATCORE	0210 0210H	-
CMU control register	STATHTRUN	0210 0300H	-
CMU control register	STATHTDBG	0210 0304H	-
CMU control register	STATHTDIS	0210 0308H	-
CMU control register	HARTRUN	0210 0310H	-
CMU control register	HARTDIS	0210 0320H	-
CMU control register	STATCCLR	0210 0400H	-
CMU control register	CTRLCCLR	0210 0410H	-
CMU control register	FUNCCTRL	0210 0600H	-
CMU control register	SSCRATCH0	0210 0700H	-
CMU control register	SSCRATCH1	0210 0704H	-
CMU control register	MONDBG	0210 0800H	-
CMU control register	MONRST	0210 0804H	-
CMU control register	MONSYS	0210 0808H	-
CMU control register	MONINT	0210 080CH	-
CMU control register	BOOTHART	0210 0900H	-
CMU control register	INITMTVEC	0210 0904H	-
CMU control register	INITRSTVEC	0210 0908H	-
CMU control register	INITNMIVEC	0210 0910H	-
CMU control register	MARCHID	0210 0FF0H	-
CMU control register	MIMPID	0210 0FF4H	-
Memory Mapped Control Register	EXCLMONVALIDBITENTRY0	0210 1000H	-
Memory Mapped Control Register	EXCLMONADDRESSENTRY0	0210 1004H	-
Memory Mapped Control Register	EXCLMONIDENTRY0	0210 1008H	-

Region	Register Name	Address 1	Address 2
Memory Mapped Control Register	EXCLMONSIDEBANDENTRY0	0210 100CH	-
Memory Mapped Control Register	EXCLMONVALIDBITENTRY1	0210 1010H	-
Memory Mapped Control Register	EXCLMONADDRESSENTRY1	0210 1014H	-
Memory Mapped Control Register	EXCLMONIDENTRY1	0210 1018H	-
Memory Mapped Control Register	EXCLMONSIDEBANDENTRY1	0210 101CH	-
Memory Mapped Control Register	LINKBIT0	0210 1100H	-
Memory Mapped Control Register	LINKADDR0	0210 1104H	-
Memory Mapped Control Register	L1CRACTRL	0210 1600H	-
Memory Mapped Control Register	L1CRATGT	0210 1604H	-
Memory Mapped Control Register	L1CRADAT0	0210 1608H	-
Memory Mapped Control Register	L1CRADAT1	0210 160CH	-
Memory Mapped Control Register	BTBACTRL	0210 1800H	-
Memory Mapped Control Register	BTBATGT	0210 1804H	-
Memory Mapped Control Register	BTBADAT	0210 1808H	-
GPIO INT	extint	E000 0000H	-
GPIO INT	extnmi	E000 0008H	-
Version Register	VERL	E1FF F000H	-
Version Register	VERH	E1FF F008H	-
SPI Select	SPISEL	E400 0000H	-
SPI Select	SPISEL.sel	E400 0000H	-
GPIO LED	LED	E400 1000H	-
GPIO LED	LEDOUT	E400 1004H	-
I2C	GIE	E400 201CH	-
I2C	ISR	E400 2020H	-
I2C	IER	E400 2028H	-
I2C	SOFTR	E400 2040H	-
I2C	CR	E400 2100H	-
I2C	SR	E400 2104H	-
I2C	TXFIFO	E400 2108H	-
I2C	RXFIFO	E400 210CH	-
I2C	ADR	E400 2110H	-
I2C	TXFIFOOCY	E400 2114H	-
I2C	RXFIFOOCY	E400 2118H	-
I2C	TENADR	E400 211CH	-
I2C	RXFIFOPIRQ	E400 2120H	-
I2C	GPO	E400 2124H	-
I2C	TSUSTA	E400 2128H	-
I2C	TSUSTO	E400 212CH	-
I2C	THDSTA	E400 2130H	-
I2C	TSUDAT	E400 2134H	-
I2C	TBUF	E400 2138H	-

Region	Register Name	Address 1	Address 2
I2C	THIGH	E400 213CH	-
I2C	TLOW	E400 2140H	-
I2C	THDDAT	E400 2144H	-
SPI XiP Control	SPIXSPICR	E400 3060H	-
SPI XiP Control	SPIXSPISR	E400 3064H	-
SPI STD Control	SPI0SRR	E400 4040H	-
SPI STD Control	SPI0SPICR	E400 4060H	-
SPI STD Control	SPI0SPISR	E400 4064H	-
SPI STD Control	SPI0SPIDTR	E400 4068H	-
SPI STD Control	SPI0SPIDRR	E400 406CH	-
SPI STD Control	SPI0SPISSR	E400 4070H	-
SPI STD Control	SPI0SPITXFOC	E400 4074H	-
SPI STD Control	SPI0SPIRXFOC	E400 4078H	-
SPI STD Control	SPI0DGIER	E400 401CH	-
SPI STD Control	SPI0IPISR	E400 4020H	-
SPI STD Control	SPI0IPIER	E400 4028H	-
SPI eMMC Control	SPI1SRR	E400 5040H	-
SPI eMMC Control	SPI1SPICR	E400 5060H	-
SPI eMMC Control	SPI1SPISR	E400 5064H	-
SPI eMMC Control	SPI1SPIDTR	E400 5068H	-
SPI eMMC Control	SPI1SPIDRR	E400 506CH	-
SPI eMMC Control	SPI1SPISSR	E400 5070H	-
SPI eMMC Control	SPI1SPITXFOC	E400 5074H	-
SPI eMMC Control	SPI1SPIRXFOC	E400 5078H	-
SPI eMMC Control	SPI1DGIER	E400 501CH	-
SPI eMMC Control	SPI1IPISR	E400 5020H	-
SPI eMMC Control	SPI1IPIER	E400 5028H	-
UART	URXFIFO	E400 6000H	-
UART	UTXFIFO	E400 6004H	-
UART	USTAT	E400 6008H	-
UART	UCTRL	E400 600CH	-

Revision History

Revision	Date	Description
1.0.0	April 18, 2022	Revision 1.0.0
1.0.1	March 7, 2023	Revision 1.0.1
2.0.0 (Preliminary)	Apr 21, 2023	Update for NS31A Rev200

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■Contact

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